Range-Scaled 14b 30 MS/s Pipeline-SAR Composite ADC for High-Performance CMOS Image Sensors

Jun-Sang Park, Jong-Min Jeong, Tai-Ji An, Gil-Cho Ahn, and Seung-Hoon Lee

Abstract—This paper proposes a low-power range-scaled 14b 30 MS/s pipeline-SAR composite ADC for high-performance CIS applications. The SAR ADC is employed in the first stage to alleviate a sampling-time mismatch as observed in the conventional SHA-free architecture. A range-scaling technique processes a wide input range of 3.0V_{pp} without thick-gate-oxide transistors under a 1.8 V supply voltage. The first- and second-stage MDACs share a single amplifier to reduce power consumption and chip area. Moreover, two separate reference voltage drivers for the first-stage SAR ADC and the remaining pipeline stages reduce a reference voltage disturbance caused by the high-speed switching noise from the SAR ADC. The measured DNL and INL of the prototype ADC in a 0.18 μm CMOS are within 0.88 LSB and 3.28 LSB, respectively. The ADC shows a maximum SNDR of 65.4 dB and SFDR of 78.9 dB at 30 MS/s, respectively. The ADC with an active die area of 1.43 mm² consumes 20.5 mW at a 1.8 V supply voltage and 30 MS/s, which corresponds to a figure-of-merit (FOM) of 0.45 pJ/conversion-step.

Index Terms—Analog-to-digital converter (ADC), range-scaling, wide input range, pipeline-SAR, separate reference

I. INTRODUCTION

Recently, with better integration capabilities and cost advantages, CMOS image sensor (CIS) has been replacing well established high-performance charge-coupled device (CCD)-based image sensor. The high-performance CIS requires the analog-to-digital converter (ADC) with a high resolution of 14b level and a wide input range to obtain a high dynamic range [1].

Meanwhile, digital single-lens reflex (DSLR) cameras require a high-end CIS with 24 Mega-pixels at a rate of 10 frame/s to retain high-definition images in a still image mode. In this case, a few high-speed high-resolution ADCs based on a multi-channel topology are more suitable than hundreds or even thousands of low-speed ADCs based on a column-parallel topology in common CIS products to minimize chip area, power consumption, and mismatch concerns such as fixed-pattern noise (FPN) between the employed ADC channels [2].

Among various ADC architectures, the pipeline is one of the best candidate architectures for a high resolution of 14b and an operating speed of tens of MS/s [3-8]. In the conventional pipeline architecture, a front-end sample-and-hold amplifier (SHA) is employed, as shown in Fig. 1(a). However, the front-end SHA needs a high-performance amplifier with a high DC gain and a high operation speed to minimize signal settling and non-linear errors of the SHA at 14b level. Thus, the front-end SHA tends to occupy a large area with considerable power consumption. To overcome these disadvantages, a SHA-free pipeline ADC has been proposed, as shown in Fig. 1(b) [9-14]. However, the SHA-free architecture suffers from a sampling-time mismatch due to a difference in input sampling paths between the first-stage multiplying digital-to-analog converter (MDAC) and the flash ADC. Although the sampling-time mismatch can be
alleviated by elaborate layout, it cannot be completely solved due to process, supply voltage, and temperature (PVT) variations [9, 11].

In the proposed pipeline successive-approximation register (pipeline-SAR) composite ADC, the SAR ADC performs the function of sampling and converting analog input signals in place of the DAC, the SHA, and the flash ADC in the first stage of the conventional pipeline ADC, as shown in Fig. 1(c). This architecture not only enhances power efficiency, but also alleviates the sampling-time mismatch.

Meanwhile, wide input range processing is also required to cover an illumination range in CIS. To process a wide input range, some previously reported ADCs employ analog circuits with thick-gate-oxide transistors and high supply voltages [3]. However, this method reduces the overall power efficiency of the ADC since analog circuits with high supply voltages consume a significant amount of power. For this reason, the proposed SAR ADC employs a range-scaling technique to properly process a wide input range of $3.0V_{pp}$ without thick-gate-oxide transistors under a 1.8 V supply voltage.

The proposed ADC minimizes power consumption and chip area by sharing a single residue amplifier for the first- and second-stage MDACs, which are the most power-hungry blocks and occupy the largest area in the conventional architecture. In addition, separate reference voltage drivers for the first-stage SAR ADC and the remaining pipeline stages reduce the reference disturbance caused by high-speed switching operation of the first-stage SAR ADC.

In the on-chip clock generator, all of the internal clocks for the proposed ADC operation are generated. The delay control circuit is integrated in the on-chip clock generator to guarantee a proper SAR conversion time affected by the PVT variations.

This work is organized as follows. The overall architecture and functions of the proposed ADC are described in Section II. The circuit design techniques for the pipeline-SAR composite ADC are discussed in Section III. The measured results of the proposed ADC are summarized in Section IV and the conclusion is given in Section V.

II. ARCHITECTURE

The proposed 14b 30 MS/s ADC employs a 4-step pipeline-SAR composite architecture, as shown in Fig. 2. The ADC consists of a range-scaled SAR ADC, three MDACs, three flash ADCs, current and voltage (I/V) references, a clock generator, and a digital correction logic (DCL) block with a decimator.

The pipeline-SAR composite topology substitutes the functions of receiving and converting an analog input signal to generate a 4b digital code and a residue signal with a SAR topology in the first stage, which considerably reduces the power consumption, circuit noise, and sampling-time mismatch of the first stage.

By employing a range-scaling technique, the first-stage SAR conversion and the following pipeline operations are based on an attenuated signal swing of $1.5V_{pp}$ for stable operation with a sufficient saturation.
margin of transistors at a 1.8 V supply voltage. Moreover, the first- and second- stage MDACs, MDAC1 and MDAC2, share a single amplifier with two separate differential input pairs to reduce power consumption and chip area [15].

The timing diagram of major functional circuit blocks such as the first-stage SAR ADC and the shared amplifier for the MDAC1 and MDAC2 is shown in Fig. 3. The first-stage SAR ADC samples an input signal during Q1X phase, while it determines a 4b digital code and generates a residue signal through the SAR conversion during Q1Y phase. The clock phase of Q1X and Q1Y, and a high-speed clock of 320 MHz for the SAR conversion are internally generated from an external 30 MHz master clock. Particularly, the duty cycles of Q1X and Q1Y can be manually controlled within 2.4ns to obtain more stable operations of sampling and SAR conversion in response to PVT variations [16]. The shared amplifier operates for the MDAC2 during every Q1 phase, and as residue amplifiers for the MDAC1 alternately during Q2 phase.

III. CIRCUIT DESCRIPTION

1. Proposed Range-scaled SAR ADC

The proposed range-scaling scheme attenuates a wide input range of 3.0V_{inp} to be processed without thick-gate-oxide transistors under a 1.8 V supply voltage, as shown in Fig. 4 in a simplified single-ended version. The first-stage range-scaled 4b SAR ADC samples an input signal only on a most significant bit (MSB) capacitor corresponding to a half of total sampling capacitors, and the other half are connected to a signal ground. The stored charge on total sampling capacitors of the SAR ADC based on the range-scaling technique is expressed in (1), where C_s and C_u indicate total sampling capacitors and a unit capacitor, respectively.

\[ Q_s = \frac{C_s}{2} \times V_{IN} = 8C_uV_{IN} \]  

The sampled input is converted successively into a 4b digital code through the SAR conversion. The charge during the SAR conversion is expressed in (2), where C_i and C_j are the sum of the capacitors connected to V_{REF} and ground, respectively.

\[ Q_C = C_i \times (V_{REF} - V_{DAC\_OUT}) + C_j \times (-V_{DAC\_OUT}) \]  

The final output voltage of the range-scaled capacitor array is derived as (3) from (1) and (2).

\[ V_{DAC\_OUT} = \frac{-V_{IN}}{2} + \frac{C_i}{16C_u} \times V_{REF} \]  

From (3), a wide input range of 3.0V_{inp} is attenuated by half. Thus, the first-stage SAR conversion and remaining pipeline operations are based on an attenuated signal range of 1.5V_{inp} with a high enough saturation margin of transistors at a 1.8 V supply voltage. Therefore, the proposed ADC needs only a single reference voltage
The first-stage SAR ADC with the range-scaling technique described above is shown in Fig. 5. The MSB capacitor, $8C_U$, is split into two units to reduce the design expense of sampling and reference switches. Considering the required 14b accuracy and the kT/C noise at a 3.0V$_{p-p}$ input signal, 6.0 pF sampling capacitors are used in the first-stage SAR ADC. To alleviate a reference disturbance problem caused by the high-speed SAR switching noise during the MDAC2 residue amplification, two reference voltages with the same level, $\pm V_{RS}$ and $\pm V_{RP}$, are produced and separated for the SAR conversion and the remaining pipeline stages, respectively. In addition, a gate-bootstrapping technique is applied to analog input switches in order to sample a wide-range input signal of 3.0V$_{p-p}$ with less distortion. While a gate-oxide breakdown voltage for device reliability is 4.6 V in this CMOS process, a maximum gate-source voltage of the bootstrapped switches is designed below a 80% level of a supply voltage during the input sampling phase.

In the proposed ADC, a clock generator is implemented on chip to generate the required internal clocks using a single external 30 MHz master clock, CLK$_{EXT}$, as shown in Fig. 6. The on-chip clock generator is composed of a main clock generator, a sub-clock generator, and a delay control circuit. The main clock generator produces 8 phases for the MDAC and the flash ADC operations while the sub-clock generator generates 5 phases for the first-stage SAR ADC operation using two of the 8 phases, Q2B and Q1PB. Among the resultant 5 phases, the input sampling phase and the SAR conversion phase, Q1X and Q1Y, are manually adjusted by a delay control circuit to obtain more stable operations of sampling and SAR conversion in response to the potential PVT variations. The delay is controlled by a specific RC time constant in 16 steps by using a 4b external digital control code. The delay interval is adjusted in a time step of 150 ps while an adjustable maximum-delay time is 2.4 ns.

The high-speed clock circuit also generates a 320 MHz clock, CK_INT, to decide a 4b digital code during Q1Y, as shown in Fig. 7. The CK_INT is generated from Q1Y, two voltage delay cells of VDL1B and VDL2, and several digital logic gates. A 3b counter aborts the clock generation by detecting the fifth rising edge of CK_INT, which indicates a completion of the SAR conversion. On the other hand, the reference sampling (RS) and the preamp amplifying (PA) time interval, $t_1$, and the time interval of CK_INT, $t_1+t_2$, can be controlled by two external 3b control pins, CNTL1<0:2> and CNTL2<0:2>, respectively, to optimize the RS, PA, and latching time in response to the PVT variations. In this work, the optimized CNTL1 and CNTL2 codes are properly traced by inspecting an off-chip signal synchronized to the fifth rising edge of CK_INT during the measurements of the prototype ADC.
2. Shared Amplifier for the MDAD1 and MDAC2

In the proposed pipeline-SAR composite ADC, a single amplifier is shared between the MDAC1 and MDAC2 to reduce power consumption and chip area. The shared amplifier employs a two-stage amplifier topology to meet a high DC gain requirement for 14b, as shown in Fig. 8.

A telescopic topology is selected for both the first- and second-stage amplifiers, AMP1 and AMP2, thereby achieving a high DC gain of 106.2 dB. In addition, two separate input pairs of the shared amplifier can be effectively reset without an extra reset timing. As a result, the conventional memory effect caused by typical amplifier-sharing techniques can be greatly reduced. The two input pairs are turned on and off alternately by two slightly overlapped clocks, Q1B and Q2B, to prevent the glitch noise and the settling time delay caused by the two input pairs turning off simultaneously [15]. Meanwhile, the shared amplifier employs a cascode compensation technique to obtain a high phase margin compared to the Miller compensation technique [17]. As a result, the amplifier achieves a phase margin of approximately 55° and a wide bandwidth of 220.9 MHz with low power consumption.

3. On-Chip I/V References with Separate Drivers

In the proposed ADC, the amplification period of the MDAC2 overlaps with the SAR conversion period, as shown in Fig. 9. If only a single reference voltage driver is used for the SAR ADC and the MDAC2, high-speed SAR switching noise can directly degrade the reference voltage settling for amplifying operation. In this case, it is difficult to settle the reference voltage within a 14b accuracy corresponding to the attenuated signal range of 1.5V_p-p. The single reference voltage driver also requires wider bandwidth and more power consumption to meet a 14b accuracy. Thus, two separate reference voltage drivers can achieve a better signal settling behavior with less power consumption while the reference disturbance is minimized.

The simulated references during SAR operation and residue amplification, respectively, are illustrated in Fig. 10, when two separate voltage drivers are employed. A maximum transient voltage noise of 38.5 mV due to high-speed SAR switching can affect directly a 14b accurate reference voltage for residue amplification, if two references are not isolated. The proposed separate reference drivers dissipate a total of 8.3 mW with a sampling rate of 30 MS/s at a supply voltage of 1.8 V, while decoupling capacitors of 70 pF are implemented on chip. On the other hand, a shared single reference driver cannot meet the required signal settling target of 14b at 30 MS/s, even with a power dissipation of 20 mW and...
decoupling capacitors of 200 pF.

The proposed on-chip I/V references with two separate drivers is illustrated in Fig. 11. To minimize a mismatch between $\pm V_{RS}$ and $\pm V_{RP}$, both of a current reference generator (IREF) and a voltage level shifter are shared while only the reference voltage drivers are divided. Current and voltage mismatches can be calibrated by a 3b digital code, IVCN<0:2>, considering various user environments, while external reference voltages can be selectively employed depending on system applications.

IV. MEASUREMENT RESULTS

The proposed 14b 30 MS/s ADC is implemented in a 0.18 $\mu$m CMOS technology. The die photo and layout of the prototype ADC is shown in Fig. 12. The prototype ADC occupies an active die area of 1.43 mm$^2$ including on-chip MOS decoupling capacitors of 980 pF in the idle space surrounded by dashed lines of Fig. 12 to reduce interferences between functional blocks, electromagnetic interference (EMI), power supply noise, and transient glitches.

The measured differential non-linearity (DNL) and integral non-linearity (INL) are 0.88 LSB and 3.28 LSB, respectively, as shown in Fig. 13. The typical FFT spectrum of the prototype ADC measured with a 3.0V_p-p input sinusoidal signal of 4 MHz at 30 MS/s is plotted in Fig. 14. This FFT spectrum is decimated by a factor of two using the on-chip decimator of the ADC. The performance degradation of INL is caused primarily by a finite gain error of amplifier and a capacitor mismatch, which is verified from the MATLAB modeling. Although the INL performance can be improved by well-known calibration schemes with some extra circuits and timing cycles, the proposed ADC does not employ any calibration technique to minimize power consumption and chip area, considering this specific CIS application.

The common noise sources to deserve consideration in the ADC design and the theoretically achievable maximum SNR in the proposed ADC are summarized in Table 1. The analysis is based on a sinusoidal input signal power, a 14b-level quantization noise power, and an input-referred thermal noise power from the kT/C noise and the amplifiers. One of the major performance-
Table 1. Primary noise sources and theoretically achievable maximum SNR of the proposed ADC

<table>
<thead>
<tr>
<th>Noise Source</th>
<th>Maximum SNR (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quantization Noise</td>
<td>52.9 uV rms</td>
</tr>
<tr>
<td>Input-referred KTC Noise</td>
<td>62.5 uV rms</td>
</tr>
<tr>
<td>Input-referred Amplifier Noise</td>
<td>400.5 uV rms</td>
</tr>
<tr>
<td>Achievable Maximum SNR</td>
<td>68.3 dB (11.1 bits)</td>
</tr>
</tbody>
</table>

Fig. 15. Measured SFDR and SNDR of the prototype ADC versus (a) sampling frequency, (b) input frequency.

limiting factors is a thermal noise of the amplifiers. In the proposed ADC, the noise and power consumption are traded off and a partially improved SNR performance can be achieved by burning more power, depending on system applications requiring a higher dynamic performance.

The measured dynamic performance of the prototype ADC is shown in Fig. 15(a) with a sampling frequency increased from 10 MS/s to 30 MS/s and a differential input frequency of 4 MHz. While the sampling frequency increases, the signal-to-noise-and-distortion ratio (SNDR) and spurious-free dynamic range (SFDR) are maintained above 65.4 dB and 78.9 dB, respectively. The SNDR and the SFDR are measured in Fig. 15(b) when an input frequency increases from 4 MHz to 15 MHz with a sampling frequency of 30 MS/s. When the input frequency increases to the Nyquist frequency at a sampling frequency of 30 MS/s, the SNDR and SFDR are maintained above 60.1 dB and 70.1 dB, respectively.

The performance of the prototype ADC is summarized in Table 2. The prototype ADC dissipates 28.8 mW including on-chip current and voltage references, and 20.5 mW excluding on-chip references, at a sampling rate of 30 MS/s and a supply voltage of 1.8 V. The prototype ADC demonstrates a competitive figure of merit (FoM) of 0.45 pJ/conversion-step, as defined in (4), without on-chip I/V references. With on-chip I/V references, the FoM is measured to be 0.63 pJ/conversion-step.

\[
FoM = \frac{\text{Power}}{2^{\text{SNDR}} \times f_s}
\]  (4)

The proposed ADC and some previously reported ADCs with a 14b resolution and a conversion rate of 30 MS/s level are compared in Table 3. Although the

Table 2. Performance summary of the prototype ADC

<table>
<thead>
<tr>
<th>Resolution</th>
<th>14 bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Speed</td>
<td>30 MS/s</td>
</tr>
<tr>
<td>Process</td>
<td>MagnaChip 0.18 μm CMOS</td>
</tr>
<tr>
<td>Supply</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Input Range</td>
<td>3.0Vp-p (Differential)</td>
</tr>
<tr>
<td>SNDR (dB)</td>
<td>65.4 @ f = 4 MHz</td>
</tr>
<tr>
<td>SFDR (dB)</td>
<td>78.9 @ f = 4 MHz</td>
</tr>
<tr>
<td>INL</td>
<td>-0.56 / +0.88 LSB</td>
</tr>
<tr>
<td>INL</td>
<td>-3.28 / +3.11 LSB</td>
</tr>
<tr>
<td>ADC Power</td>
<td>28.8 mW</td>
</tr>
<tr>
<td>FoM</td>
<td>0.63 pJ/Conv.</td>
</tr>
<tr>
<td>Die Area</td>
<td>1.43 mm (= 1.1 mm × 1.3 mm)</td>
</tr>
</tbody>
</table>

Table 3. Performance comparison of the proposed ADC and previously reported ADCs with 14b 30MS/s level

<table>
<thead>
<tr>
<th>This Work</th>
<th>[18]</th>
<th>[19]</th>
<th>[3]</th>
<th>[20]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Speed (MS/s)</td>
<td>30</td>
<td>23</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>Supply Voltage (V)</td>
<td>1.8</td>
<td>2</td>
<td>1.2</td>
<td>3.3/1.0</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>20.5</td>
<td>48.0</td>
<td>2.5</td>
<td>106</td>
</tr>
<tr>
<td>SNDR (dB)</td>
<td>65.4</td>
<td>72.0</td>
<td>70.4</td>
<td>69.3</td>
</tr>
<tr>
<td>FoM (pJ/Conv.)</td>
<td>0.45</td>
<td>1.02</td>
<td>0.03</td>
<td>1.48</td>
</tr>
<tr>
<td>Input Range (Vp-p)</td>
<td>3.0</td>
<td>2.0</td>
<td>2.0</td>
<td>-</td>
</tr>
<tr>
<td>Thick-gate-oxide Transistor</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>O</td>
</tr>
<tr>
<td>Calibration</td>
<td>X</td>
<td>X</td>
<td>O</td>
<td>O</td>
</tr>
<tr>
<td>Process (CMOS)</td>
<td>0.18 μm</td>
<td>0.18 μm</td>
<td>0.13 μm</td>
<td>90 nm</td>
</tr>
</tbody>
</table>

...
prototype ADC is implemented with only nominal-gate-oxide thickness transistors in a 0.18 μm CMOS technology, it can process quite wide input range without thick-gate-oxide transistors and any calibration schemes. The proposed ADC demonstrates the lowest FoM performance except [19].

V. CONCLUSIONS

This paper describes a 14b 30 MS/s 0.18 μm CMOS pipeline-SAR composite ADC based on a range-scaling scheme to properly process a wide input range of 3.0Vp.p with high power efficiency for various CIS applications. The proposed ADC minimizes a sampling-time mismatch as observed in the conventional SHA-free ADC topology by substituting the function of receiving and converting analog input signals with a SAR topology in the first stage. The proposed range-scaling technique is employed in the SAR ADC to process a wide-range input signal of 3.0Vp.p using only 1.8 V devices of a 0.18 μm CMOS technology without thick-gate-oxide transistors. A shared amplifier for the first- and second-stage residue amplification reduces power consumption and chip area. The reference voltage driver for the first-stage SAR ADC is separated from the other driver for the remaining pipeline stages to minimize the reference disturbance. A delay circuit in the proposed on-chip clock generator controls both of the clock duty cycle and time interval for the SAR ADC while guaranteeing a proper SAR conversion time degraded by PVT variations. The prototype ADC occupies an active die area of 1.43 mm², and the measured maximum DNL and INL are 0.88 LSB and 3.28 LSB, respectively. The maximum SNDR and SFDR are 65.4 dB and 78.9 dB, respectively, at a 30 MS/s sampling speed with a 4 MHz input signal. A power consumption of the prototype ADC is 28.8 mW at a 1.8 V supply voltage including on-chip I/V references, and 20.5 mW excluding on-chip I/V references. The prototype ADC demonstrates a FoM of 0.63 pJ and 0.45 pJ/conversion-step with and without on-chip references, respectively.

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Seung-Hoon Lee received the B.S. and M.S. degrees in electronic engineering from Seoul National University, Korea, in 1984 and 1986, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Illinois, Urbana-Champaign, in 1991. He was with Analog Devices Semiconductor, Wilmington, MA, from 1990 to 1993, as a Senior Design Engineer. Since 1993, he has been with the Department of Electronic Engineering, Sogang University, Seoul, where he is currently a Professor. His current research interests include design and testing of high-resolution high-speed CMOS data converters, CMOS communication circuits, integrated sensors, and mixed-mode integrated systems. Dr. Lee has been a member of the editorial board and the technical program committee of many international and domestic journals and conferences including the IEEK Journal of Semiconductor Devices, Circuits, and Systems, the IEICE Transactions on Electronics, and the IEEE Symposium on VLSI Circuits. Since 2006, he has been organizing various industry-university mutual cooperative programs with many companies such as Samsung Electronics, SK Hynix, and LG Electronics. In 2010, he founded Analog IP Research Center supported by the Ministry of Science, ICT&Future Planning, Korea.